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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/032,289 | 12/21/2001 | Sergio Tommaso Spampinato | 853063.497 | 4035 |

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| EXAMINER | |
|---|---|
| FARAHANI, DANA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 07/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Advisory Action | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/032,289 | SPAMPINATO, SERGIO TOMMASO | |
| | Examiner | Art Unit | |
| | Dana Farahani | 2814 | |

*--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

THE REPLY FILED 29 June 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ they raise the issue of new matter (see Note below);
   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____.
3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.
8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s)( PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

Continuation of 5. does NOT place the application in condition for allowance because: note that in the Aiello reference the use of monocrystalline structure is not critical to the device. Therefore, it would have been obvious to replace the strucutre with polysilicon to get faster performing transistors in the structure (see Yi et al., column 1, lines 25-27) .

LONG PHAM
PRIMARY EXAMINER

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 38 recites the limitation "the first zone" and "the second zone " in the last four lines. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6-14, 23-26, 31, 32, and 34-43 are rejected under 35 U.S.C. 103(a) as being anticipated by Aiello et al., hereinafter Aiello (U.S. Patent 6,127,723), in view of Yi et al., hereinafter Yi (U.S. Patent 6,207,481), all previously cited

Regarding claims 1, 6-8, 14, and 31, Aiello discloses in figure 2a an Integrated device being integrated in a chip of semiconductor material 218 of a first conductivity type, said chip having a first (lower) surface and a second (upper) surface opposite to each other, said device comprising a first transistor Td1 having a base region (242), an emitter region (251) and a collector region; a second transistor (comprising regions 218, 209, and 206 ) which is connected with the first transistor; a quenching element (pn junction of 242 and 218) of the first transistor, which discharges current there from when

said second transistor is turned off, said quenching element being coupled with the base terminal of the first transistor and with the other not drivable terminal of the second transistor, said quenching element having at least one Zener diode, said at least one Zener diode being formed on the second surface of said chip and comprising a layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction.

Aiello does not disclose the zener diode is a polysilicon.

Yi discloses a transistor, wherein it teaches using polysilicon results in uniform crystal size and a better transistor performance. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use polysilicon in Aiello's structure, as Yi teaches, since using polysilicon is advantageous, as mentioned above.

Regarding claim 2, the chip comprises a first region 242 of the second conductivity type which extends from the second surface into the chip and a second region 251 of the first conductivity type which extends from the second surface into the first region, and the first region, the second region and a portion of the chip comprised between the first region and the first surface forming respectively the base region, the emitter region and the collector region of the first transistor.

Regarding claim 3, the first transistor and said second transistor are bipolar transistors and said chip comprises a third region 209 of the second conductivity type which extends from the second surface into the second region and a fourth region 218 of the first conductivity type which extends from the second surface into the third region,

each of the first region, of the third region and of the fourth region forming respectively the collector region, the base region and the emitter region of the second transistor.

Regarding claims 4 and 40, a third bipolar transistor Td2 connected with the first transistor in a Darlington configuration and the collector terminal of the first transistor is connected with the collector terminal of the third transistor.

Regarding claims 9-12, 41, and 42, the at least one polysilicon Zener diode comprises first and second polysilicon Zener diodes (one comprises regions 242 and 218; and the other is 209 and 206. Similarly, there are plurality of diodes corresponding to regions 239, 242 and 245) in back to back connection wherein the anode of the first Zener diode is connected with the anode of the second Zener diode and the cathode of the first Zener diode is connected with the base terminal of the first transistor and the cathode of the second Zener diode is connected with said other not drivable terminal of the second transistor.

Regarding claim 13, region 257 of figure 2a is an insulating layer (see column 3, line 50).

Regarding claims 23-26, 32, and 43, Aiello discloses the limitations in the claims, as above discussed, further disclosing insulating layer 257 and polysilicon layer 218 on the insulating layer.

Regarding claims 5 and 39, Aiello discloses in figure 4a MOS transistor Me, third and fourth regions 410 and 420, respectively. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make a MOS transistor in

the embodiment of figure 2a in order to make the emitting-switching structure of figure 4b.

Regarding claim 34, Aiello discloses in figure 2a, a chip of semiconductor material, the chip having a first surface and a second surface opposite to each other, the device comprising a first transistor, Td1, having a control region 242 and first and second conduction regions, 251 and the region directly below region 242, respectively, a second transistor, Td2, having a control region 245 and first and second conduction regions, 254 and the region directly below region 245, respectively, the first conduction region of the second transistor being connected to the second conduction region of the first transistor, as can be seen in the figure; and quenching means D1, the quenching means being connected between the control terminal of the first transistor and the second conduction region of the second transistor, and including a first zone of the first conductivity type and a second zone of a second conductivity type in order to form a first P-N junction, shown in the figure.

Regarding claim 35, Aiello discloses in figure 2a the control region of the second transistor includes a first region 242 of the second conductivity type that extends from the second surface (top) into the chip, the second conduction region of the second transistor includes a second region 218 of the first conductivity type the extends from the second surface into the first region, and the first conduction region of the second transistor includes a third region 254 of the first conductivity type positioned between the first region and the first surface.

Regarding claim 36, the first transistor and the second transistor in figure 2a are bipolar transistors, the second conduction region (218) of the first transistor includes the third region (254), the first conduction terminal 251 of the first transistor includes a portion of the chip between the third region and the first surface, as can be seen in the figure, and the control region 242 of the first transistor includes a fourth region 242 positioned between the third region 254 and the portion of the chip between the third region and the first surface, as can be seen in the figure.

Regarding claim 37, note that a first transistor also could have been consisted of regions 218, 209 (second buried region) and 215 (first buried region), wherein the second conduction region is 218, and the transistor control region are regions 209 and 221. In this case, Td1 is the second transistor, and Td2 is the third transistor.

Regarding claim 38, the second conduction region 218 of the second transistor includes a region 236 of the first conductivity type extending from the top surface into the chip, the device further comprising a sinker region 221 that extends from the second surface, or top surface of the chip into the second buried region 209.

5. Claims 33 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiello in view of Yi as applied to claim 1 above, and further in view of Kato et al., hereinafter Kato (US Patent 4,994,880).

Aiello in view of Yi renders obvious the claimed invention, as discussed above, except for the emitter region of the first transistor extends as a comb shape.

Kato discloses in figure 8A, emitter surface electrode 47 is in a comb shape. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to use a comb shape emitter in order to save space on the semiconductor chip.

***Response to Arguments***

6. Applicant's arguments filed on 12/9/03 have been fully considered but they are not persuasive.

Applicant argues that there is no motivation to combine the primary and the secondary reference. Note that the Yi reference is merely cited to show the obviousness of interchanging a monocrystalline material with a polycrystalline one. The Yi reference has not been structurally combined in any way with the primary reference, and it is cited to show that it is within the level of ordinary skill in the art to use either a polycrystalline or a monocrystalline material. Furthermore, case laws make it clear that choosing an appropriate material is in fact within the level of ordinary skill in the art.

Applicant further argues that the limitation in claim 1, namely, the diode is connected with the base region of the first transistor and with the not drivable terminal of the second transistor is not in the references. As discussed in the above rejections, diode D1 has such connections to transistors Td1 and Td2 (or, alternatively, Td1, and the transistor comprising regions 218, 209 and 215). See figure 2b, Also.

***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
March 27, 2004

LONG PHAM
PRIMARY EXAMINER